What is claimed is:

1. A method of fabrication of doped regions in a semiconductor device; comprising the steps of :

a) providing a {001} silicon substrate;

b) forming a gate over said silicon substrate; said gate having a width and a length; a channel under the gate; said channel having a channel direction parallel with the direction of said gate width; said channel direction is [100] or [010] direction;

c) implanting ions into said silicon substrate to form a doped region adjacent to said gate; the implantation of ions comprises a large angle tilt implant with a twist of between about 40 and 50 degrees and a tilt angle of 40 and 50 degrees.

2. The method of claim 1 wherein said doped region is a N- LDD in an offset LDMOS FET.

3. The method claim 1 wherein said ions being implanted about along the [110] directions of the silicon substrate.

4. The method claim 1 wherein the implanting of said ions is performed in one implant step at an about 45 degree twist implant and a tilt angle of about 45 degrees.

5. The method claim 1 wherein said silicon substrate has a notch/flat at a [110] direction.

6. The method claim 1 wherein the implanting of ion further comprises: said silicon substrate has a notch/flat at a <110> direction,

the implantation comprises an implant with a 45 tilt and 45 twist and the ions enter the substrate aligned at a <0 -1 -1> direction whereby the direction increases the channeling.

7. The method claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel and a second doped region surrounding the outside of said channel.

8. The method claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel region and a second doped region surrounding the outside of said channel;

and the implanting of said ions further comprises a quadra implant at the twist angles of about 45, 135, 225 and 315 degrees with a range of +/- 5 degrees; and a tilt angle between 40 and 50 degrees.

9. The method claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel and a second doped region surrounding the outside of said channel region;

and the implanting of said ions further comprises a quadra implant with the ion beams aligned with the <110> direction within plus/minus 2 degrees.

10. The method claim 1 which further includes forming a High Vt NMOS FET from said gate and doped regions.

11. The semiconductor device of claim 1 wherein a LDMOS device is formed.

12. The semiconductor device of claim 1 which further comprises forming a second gate over said silicon substrate; said second gate having a width and a length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the <110> direction.

13. A semiconductor device at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:

a {001} silicon substrate having ;

a gate having a length and a width; said gate having the gate width in the [100] or [010] crystal directions;

a source on one side of said patterned gate width and a drain on the other side of the patterned gate width, with impurities of the source and drain being disposed in the silicon substrate;

a channel under the gate between the source and drain when voltage is applied and being aligned in a direction parallel with the direction of the gate width, whereby the performance of the FET is enhanced.

14. The semiconductor device of claim 13 which further comprises said channel has an annular shape.

15. The semiconductor device of claim 13 which further comprises forming a second gate over said silicon substrate; said second gate having a width and a length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the <110> direction.

16. The semiconductor device of claim 13 wherein a LDMOS device is formed.

17. In an integrated circuit with at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:

a {100} monocrystalline silicon substrate having (100) and (110) crystal planes and [100] and [110] crystal directions;

a FET gate having a length and a width and being insulated from the substrate by a gate dielectric layer, said gate being patterned with the gate width in the [100] crystal direction so that the gate width aligned approximately orthogonal to the (100) crystal plane and parallel with the [100] crystal direction;

a source on one side of said patterned gate width and a drain on the other side of the patterned gate width, and

a channel region being formed under the gate between the source and

drain when voltage is applied and being aligned in a direction parallel with the direction of the gate width.

18. The integrated circuit of claim 17 wherein the said channel has an annular shape with either said source or said drain surrounding the outside of said channel region.

19. The integrated circuit of claim 17 which further comprises forming a second FET over said silicon substrate, said second FET comprised of a second gate over said silicon substrate; said second gate having a width and a length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the <110> direction.

20. The integrated circuit of claim 17 wherein said silicon substrate has a notch/flat at a [110] direction.

21. The integrated circuit of claim 17 wherein a LDMOS device is formed.

22. A semiconductor device comprising at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by an annular channel under the gate, comprising:

a first S/D doped region in a substrate;

a second annular S/D doped region spaced from said first S/D doped region by a channel region in said substrate;

a gate over said annular channel region; said gate has an annular shape;

23. The semiconductor device of claim 24 wherein annular channel and said second annular S/D doped region have a rectangular shape.

24. The semiconductor device of claim 24 wherein said substrate comprises a {001} monocrystalline silicon substrate;

said channel region aligned with or perpendicular with the [110] crystal direction.

25. The semiconductor device of claim 24 wherein said substrate comprises a {001} monocrystalline silicon substrate having [110] reference direction from substrate center to primary notch/flat;

said annular channel region aligned with or perpendicular with the [110] crystal direction.

26. The semiconductor device of claim 24 which further includes a first LLD region adjacent to said gate and said first S/D region; and a second LDD region having an annular shape adjacent to said second annular S/D region.

27. A method for a semiconductor device comprising at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by an annular channel under the gate, comprising:

a) forming a gate over a substrate; said gate has an annular shape; a annular channel region in said substrate under said gate;

b) forming a first S/D doped region and a second annular S/D doped region in said substrate; said second annular S/D doped region spaced from said first S/D doped region by a channel region in said substrate.

28. The method of claim 27 wherein said annular channel region and said second annular S/D doped region have a rectangular shape.

29. The method of claim 27 wherein said substrate comprises a {001} monocrystalline silicon substrate ;

said channel region aligned with or perpendicular with the [110] crystal direction.

30. The method of claim 27 wherein said substrate comprises a {001} monocrystalline silicon substrate having [110] reference direction from substrate center to primary notch/flat;

said annular channel region aligned with or perpendicular with the [110] crystal direction.

31. The method of claim 27 wherein which further includes a first LLD region adjacent to said gate and said first S/D doped region; and a second LDD region having an annular shape adjacent to said second annular S/D doped region.

32. The method claim 27 wherein said first S/D doped region and said second annualar S/D doped region form by ions being implanted about along the [110] directions of the silicon substrate.

33. The method claim 27 wherein said first S/D doped region and said second annular S/D doped region form by implanting ions in one implant step at an about 45 degree twist implant and a tilt angle of about 45 degrees.

34. The method claim 27 wherein said first S/D doped region and said second annular S/D doped region form by ions being implanted comprising a quadra implant at the twist angles of about 45, 135, 225 and 315 degrees with a range of +/- 5 degrees; and a tilt angle between 40 and 50 degrees.

35. A semiconductor device comprising at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:

a first annular S/D doped region in a substrate;

a second annular S/D doped region spaced from said first annular first annular S/D doped region by a channel region in said substrate;

said first and said second annular diffusion have a rectangular shape;

a gate over said channel region.

36. The semiconductor device of claim 35 wherein said substrate comprises a {001} monocrystalline silicon substrate;

said channel region aligned with or perpendicular with the [110] crystal direction.

37. The semiconductor device of claim 35 wherein said substrate comprises a {001} monocrystalline silicon substrate having [110] reference direction from substrate center to primary notch/flat;

said channel region aligned with or perpendicular with the [110] crystal direction.

38. A method to form a Offset LDMOS Tx by implanting the N-LDD to increase channeling comprising the steps of:

forming p-epi layer over substrate;

forming a p-well in said p- epi layer;

forming a gate dielectric and a gate over said p- epi layer; said gate having a width and a length; a channel under the gate; said channel having a channel direction parallel with the direction of said gate width; said channel direction is [100] or [010] direction;

forming a drain N-LDD region on one said of said gate; said N- LDD region form by implanting ions into said p-epi layer; the implantation of ions comprises a large angle tilt implant with a twist of between about 40 and 50 degrees and a tilt angle of 40 and 50 degrees.

forming spacers on gate; said spacers extending over said p-epi layer longer in the direction of a subsequently formed source;

forming source and drain region adjacent to said gate.

39. The method claim 38 wherein said channel has an annular shape with a source or drain region on the inside of said channel and said source or drain region surrounding the outside of said channel region.